29/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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03053238 **Image available**
METHOD FOR SUBSTITUTING BLOCK OF MULTI-HIERARCHY **CACHE** MEMORY

PUB. NO.: 02-028738 [JP 2028738 A]
PUBLISHED: January 30, 1990 (19900130)
INVENTOR(s): SHIOZAWA TSUNEMICHI
APPLICANT(s): NIPPON TELEGR & TELEPH CORP <NTT> [000422] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-178870 [JP 88178870]
FILED: July 18, 1988 (19880718)
INTL CLASS: [5] G06F-012/08; G06F-012/12
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)
JOURNAL: Section: P, Section No. 1034, Vol. 14, No. 179, Pg. 84, April 10, 1990 (19900410)

ABSTRACT

PURPOSE: To store new blocks in an order which is requested from a processor in a low-level **cache** memory by segmenting the blocks of the low-level **cache** memory in accordance with the storage state of the low-level **cache** memory.
CONSTITUTION: When a block request is given to a **cache** memory 3 in level '1' as the **cache** memory of the low-level, a **cache** memory 2 in **level** '0' as the **cache** memory of a high-level **simultaneously** gives the notice of a block which is to be substituted by said block. Thus, the blocks can be segmented to these stored in the memory 2, and those which are not stored in the memory 3. When the blocks are substituted, the memory 3 sets only the blocks which are not included in the memory 2 to be the object of substitution, and stores the new blocks in the order which the processor has requested. Consequently, the blocks are substituted in the memory 3 in the same way as a case when there is not memory 2, and the new block which the processor has requested can be taken priority and stored in an internal part.

29/5/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO
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01648250 **Image available**
CACHE MEMORY DEVICE

PUB. NO.: 60-126750 [JP 60126750 A]
PUBLISHED: July 06, 1985 (19850706)
INVENTOR(s): KUNO KIYOSHI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 58-234227 [JP 83234227]
FILED: December 14, 1983 (19831214)
INTL CLASS: [4] G06F-012/08
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)
JOURNAL: Section: P, Section No. 405, Vol. 09, No. 289, Pg. 15, November 15, 1985 (19851115)

ABSTRACT

PURPOSE: To select the write system corresponding to the system environment by providing a selection means for selecting any of a **simultaneous** write circuit and a sequential write circuit depending on the command of a high-order device.
CONSTITUTION: When a CPU1 is a system to process of a batch system, the CPU1 outputs a **0 level** signal as a control signal 5. A write data from the CPU1 is transferred to an external storage device 4 as the result that a write data from the CPU1 and a signal of level 1 inverted by a NOT circuit 6 are inputted to an AND circuit 8. Moreover, the write data is transferred to a **cache** memory section 3 at the **same time** . When the

CPU1 is the time sharing system, the signal 5 goes to level 1. A **0 level** signal is inputted from the circuit 6 to the circuit 6 to the circuit 8, resulting that the write data from the CPU1 is transferred only to a memory section 3. After the write data transfer to the device 4 is stored once in the memory section 3, the write data is transferred by an AND circuit 7 when **cache** memory devices 2 and 5 are both free.

29/5/3 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014020361 **Image available**
WPI Acc No: 2001-504575/200156
XRPX Acc No: N01-374331
Method for controlling multi-layer cache **access in which a pre- memory access step is undertaken in which the** cache **layers are accessed in** parallel **to determine if one** cache **layer is sufficient, making** cache **access more efficient**
Patent Assignee: HEWLETT-PACKARD CO (HEWP)
Inventor: DELANO E; LYON T L; MULLA D A; DELANO E R
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
FR 2804770	A1	20010810	FR 200012199	A	20000926	200156	B
US 6427188	B1	20020730	US 2000501396	A	20000209	200254	

Priority Applications (No Type Date): US 2000501396 A 20000209
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
FR 2804770	A1		38	G06F-012/08	
US 6427188	B1			G06F-012/00	

Abstract (Basic): FR 2804770 A1
NOVELTY - Method has the following steps: a command is received for access to a multi-layer **cache** memory at which point it is determined (12, 16, 24, 28) if the required memory access can be satisfied by a single layer (14, 26), with the determination being made by a **parallel** access to the multiple layer. Finally the memory access is satisfied by one layer if it has been determined by the previous step that this is possible.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are made for a computer system using a multi-layer **cache** memory according to the above method and a for a **cache** memory for access using the above method.
USE - Multi-layer **cache** memory for computer system use.
ADVANTAGE - By accessing only the required layer of **cache** , **cache** memory is speeded up along with the speed of the computer system.
DESCRIPTION OF DRAWING(S) - (Drawing includes non-English language text). Figure shows a block diagram of multi-layer **cache** memory access according to the invention.
multi-layer **cache** memory (26)
data for **L0 cache** layer (14)
circuit blocks for determining if memory requirement can be satisfied by one layer. (12, 16, 24, 28)
pp; 38 DwgNo 2/2
Title Terms: METHOD; CONTROL; MULTI; LAYER; **CACHE** ; ACCESS; PRE; MEMORY; ACCESS; STEP; **CACHE** ; LAYER; ACCESS; **PARALLEL** ; DETERMINE; ONE; **CACHE** ; LAYER; SUFFICIENT; **CACHE** ; ACCESS; MORE; EFFICIENCY
Derwent Class: T01
International Patent Class (Main): G06F-012/00; G06F-012/08
File Segment: EPI

29/5/4 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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013904487 **Image available**
WPI Acc No: 2001-388700/200141

XRPX Acc No: N01-285784
Memory accessing method for data processing system, involves retrieving information from both cache **when there is hits in both in response to memory request and ignoring information retrieved from secondary** cache
Patent Assignee: INTEL CORP (ITLC)
Inventor: BAWEJA G D; CHANG C; KUMAR H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6237064	B1	20010522	US 9827539	A	19980223	200141	B

Priority Applications (No Type Date): US 9827539 A 19980223
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6237064	B1		7	G06F-012/00	

Abstract (Basic): US 6237064 B1
NOVELTY - A memory request is issued to both the **caches** (**L0** ,L1) at the **same time** . The information is retrieved from both **caches** (**L0** ,L1), when there is hits in both in response to the memory request and the information retrieved from the **cache** (L1) is ignored.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(a) Memory accessing apparatus;
(b) Computer system
USE - For accessing memory of data processing system.
ADVANTAGE - Reduces **cache** latency without queue by implementing similar control logic elsewhere in the **cache** memory architecture.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of memory accessing apparatus.
Caches (**L0** ,L1)
pp; 7 DwgNo 1/2
Title Terms: MEMORY; ACCESS; METHOD; DATA; PROCESS; SYSTEM; RETRIEVAL; INFORMATION; **CACHE** ; HIT; RESPOND; MEMORY; REQUEST; IGNORING; INFORMATION; RETRIEVAL; SECONDARY; **CACHE**
Derwent Class: T01
International Patent Class (Main): G06F-012/00
International Patent Class (Additional): G06F-012/08
File Segment: EPI

29/5/5 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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011026287 **Image available**
WPI Acc No: 1997-004211/199701
XRPX Acc No: N97-003777
Synchronous **semiconductor memory unit e.g. file register,** cache **RAM, command memory, data memory - has PMOS transistor which provides precharge to bit line, based on precharge and control signal from external**
Patent Assignee: OKI ELECTRIC IND CO LTD (OKID)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 8273358	A	19961018	JP 9573280	A	19950330	199701	B

Priority Applications (No Type Date): JP 9573280 A 19950330
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8273358	A		11	G11C-011/409	

Abstract (Basic): JP 8273358 A
The memory unit includes a NAND gate (10) to which a control signal (RAME) and a precharge signal (phi) are fed. When both the signals are at logic `1' level, the output of the NAND gate turns a PMOS transistor (7) ON. Precharging of bit line (BL) is thus carried out.

Data held in RAM cell (1), which is connected to selected word line (WL1) is read to the bit line. The bit line then carries out a discharge. When the control signal is at logic ` **0** ' **level** , the PMOS transistor is not turned on inspite of the precharge signal being at logic `1'. Consequently, bit line discharge is not carried out, even when word line is selected.

ADVANTAGE - Reduces amount of current consumed in bit line.

Dwg.1/10

Title Terms: **SYNCHRONOUS** ; SEMICONDUCTOR; MEMORY; UNIT; FILE; REGISTER; **CACHE** ; RAM; COMMAND; MEMORY; DATA; MEMORY; TRANSISTOR; PRECHARGED; BIT; LINE; BASED; PRECHARGED; CONTROL; SIGNAL; EXTERNAL

Derwent Class: U14

International Patent Class (Main): G11C-011/409

File Segment: EPI

29/5/6 (Item 4 from file: 350)

DIALOG(R)File 350:Derwent WPIX

007929483

WPI Acc No: 1989-194595/198927

XRPX Acc No: N89-148813

Three-dimensional display of objects digitally encoded as tree - uses geometric processor unit and image generation circuit to process image data held in octree format

Patent Assignee: GENERAL ELECTRIC CGR SA (CGRR); THOMSON-CGR (CSFC)

Inventor: DELCROIX M; EDWARDS B; LIS O; MEAGHER D; MILON D; PREVOST G; MEAGNER D

Number of Countries: 008 Number of Patents: 007

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 323302	A	19890705	EP 88403179	A	19881214	198927	B
FR 2625345	A	19890630				198934	
EP 323302	B1	19920617	EP 88403179	A	19881214	199225	
US 5123084	A	19920616	US 88289380	A	19881223	199227	
			US 90630782	A	19901221		
DE 3872203	G	19920723	DE 3872203	A	19881214	199231	
			EP 88403179	A	19881214		
ES 2033457	T3	19930316	EP 88403179	A	19881214	199322	
JP 3252904	B2	20020204	JP 88325680	A	19881223	200211	

Priority Applications (No Type Date): FR 8718151 A 19871224

Cited Patents: 4.Jnl.Ref; EP 152741; WO 8002210

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 323302	A	F	37		
Designated States (Regional): DE ES GB IT NL					
EP 323302	B1	F	41	G06F-015/72	
Designated States (Regional): DE ES GB IT NL					
US 5123084	A		34	G06F-015/62	Cont of application US 88289380
DE 3872203	G			G06F-015/72	Based on patent EP 323302
ES 2033457	T3			G06F-015/72	Based on patent EP 323302
JP 3252904	B2		33	G06T-015/00	Previous Publ. patent JP 1216490

Abstract (Basic): EP 323302 A

The display system works on object data held as a tree structure which is held in a memory (28) associated with a **cache** (29) delivering blocks of data over a bus to which is connected a geometric processor (30) and an image generation circuit (31). The display system operates with an object universe and a target universe and controls the generation of images of one universe in the other universe, controlling overlay and shadowing. The geometric processor generates the visible part of a tree corresponding to a target universe which can be positioned in any manner relative to the object universe.

USE/ADVANTAGE - High speed generation of external views, shaded or not and of section views of three-dimensional images, with particular application to medical imaging.